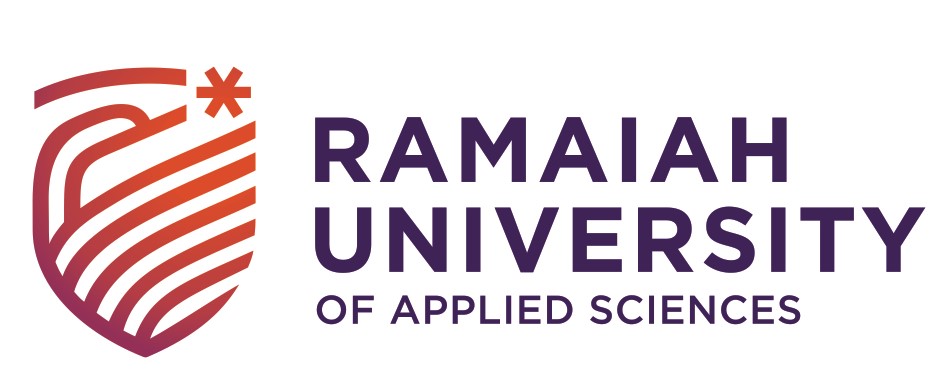
**LABORATORY RECORD**

**Course:** Logic Design Laboratory

**Semester/Batch:** 3rd Semester 2018 Batch

**Department:** Computer Science and Engineering

**Faculty:** Faculty of Engineering and Technology



**Submitted By**

**Name: TANISHQ PORWAR Semester and Section: 3RD / C-SECTION**

**Registration Number: 18ETCS002131 Staff in-charge:**

**INDEX SHEET**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Sl. No.** | **Name of Experiment** | **Conduction**  **(10)** | **Document**  **(5)** | **Total**  **(15)** | **Submitted On** | **Staff**  **Sign** |
| **1** | Introduction to Logisim and Circuit Development |  |  |  |  |  |
| **2** | Boolean Expressions using Universal Gates |  |  |  |  |  |
| **3** | Gate Level Minimization using Karnaugh Maps |  |  |  |  |  |
| **4** | Code Conversion Circuits |  |  |  |  |  |
| **5a** | Combinational Circuits-I: Adders and Subtractors |  |  |  |  |  |
| **5b** | Combinational Circuits-II: Comparators |  |  |  |  |  |
| **6** | Combinational Circuits-III: Multiplexers and Demultiplexers |  |  |  |  |  |
| **7** | Combinational Circuits-IV: Encoders and Decoders |  |  |  |  |  |
| **8** | Sequential Circuits-I: Latches and Flip Flops |  |  |  |  |  |
| **9** | Sequential Circuits-II: Universal Shift Register |  |  |  |  |  |
| **10** | Sequential Circuits-III: Asynchronous and Synchronous Counters |  |  |  |  |  |

|  |  |
| --- | --- |
| Average Marks of all experiments (Max. Marks 15) |  |
| Lab Internal Test conducted along the lines of SEE and Viva (Max. Marks 10) |  |
| **Component 1 Marks (Max. Marks 25)** |  |

**Signature of the Staff In-charge**